HW9

Wednesday, September 16, 2009
10:40 AM

Part A

(1) There are two outputs (0 and 1)
So, two states, 0 and 1 should suffice.
Hence, one FF is needed.

We will connect the final output directly to the output of the FF. (In which case, no additional circuit is needed to convert the FF's output into the final output.)

The "next-state" table can be read off from the state diagram.

Input W	Current State Q	Next State Q^*
0	0	1
0	1	1
1	0	0
1	1	0

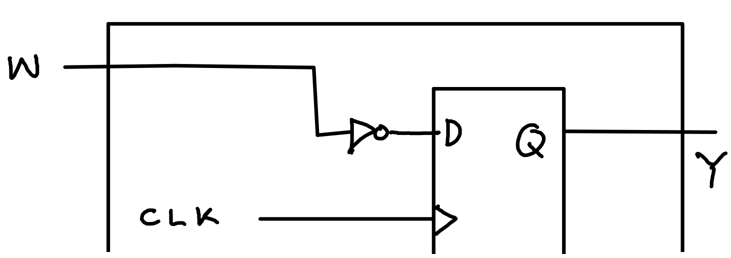
The question specifies that we have to use D FF.

For D FF, $Q^* = D$.

From the next state table we observe that

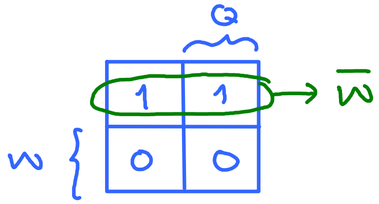
$$Q^* = \overline{W}$$ ← We want to express Q^* as a funtion of W, Q.

Therefore, the circuit that we want can be construct by putting $\overline{W}$ into the D input of the FF as shown below



Ans

Alternatively, in case that you are not sure whether you can simplify $Q^* = \overline{W}$ any further, you can use the K-map.



The K-map gives the same answer: $Q^* = \overline{W}$

(2) Note that in this question, the state diagram is exactly the same as in question (1).

The difference is that the outputs value are now 13 and 1 instead of 0 and 1

where

$$13 = \overset{Y_3 Y_2 Y_1 Y_0}{1101_2}$$
$$1 = 0001_2$$

The actual output has 4 bits.

Using what we have from question (1), we can transform our answer as followed:

we add one more box after the FF to convert the answer (Q) into the correct output value $(Y_3 Y_2 Y_1 Y_0)$.

The truth table for this box is

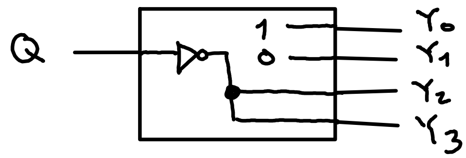
Input Q	Output Y_3	Y_2	Y_1	Y_0
0	1	1	0	1
1	0	0	0	1

$\Downarrow$ $\Downarrow$ $\Downarrow$ $\Downarrow$

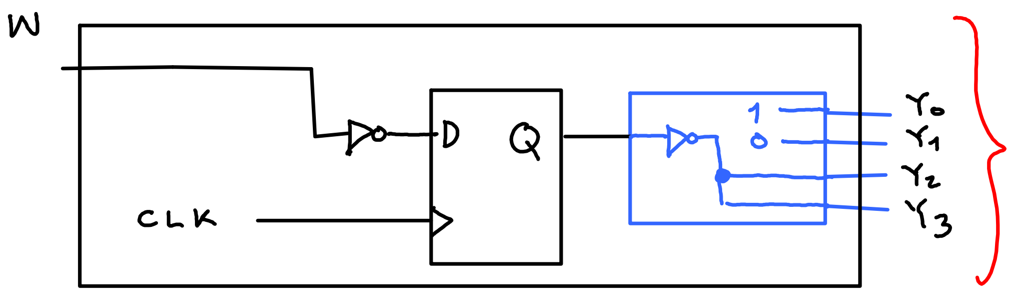
$Y_1 = 0$ $Y_0 = 1$

$$Y_3 = Y_2 = \overline{Q}$$

So, the connection inside the extra box is:



Putting this extra box after the circuit that we have from question 1 gives:



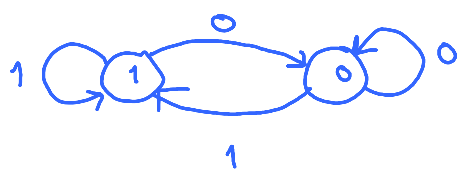
Ans

Alternatively, you may redesign the circuit from the beginning.

In which case, you have the option of whether to map 13 and 1 to 0 and 1 as what we did earlier or map 13 and 1 to 1 and 0.

Because we have already done the first mapping above, I want to show what you will get using the second mapping.

For the second mapping, the state diagram becomes



So, the next state table is

w	Q	Q^*

W	Q	Q^*
0	0	0
0	1	0
1	0	1
1	1	1

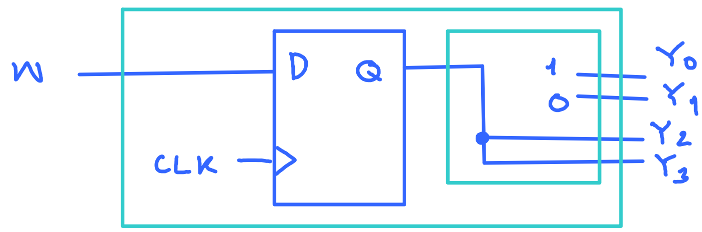
Hence, $Q^* = W$. ← This is what we will connect to the D input of the FF.

The truth table for the extra box is:

Q	Y_3	Y_2	Y_1	Y_0
0	0	0	0	1
1	1	1	0	1

$Y_3 = Y_2 = Q$ $\quad Y_1 = 0$ $\quad Y_0 = 1$

Our final answer is the following circuit



Ans (Alternative one)

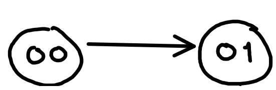
③ For this question, there are four states in the state diagram. So, we need 2 bits to specify the states. Therefore, two FFs are needed.

The question specifies that the two FFs should be one D FF and one JK FF. Moreover, we are required to have

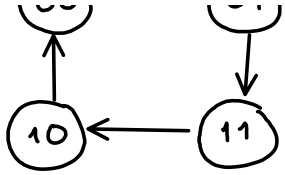
$Y_0 = Q_{JK}$ ← output of the JK FF.

$Y_1 = Q_D$ ← output of the D FF.

The state transition diagram (with state values substituted by binary values of the outputs) is as followed



Note that
there is no input



there is no input to this circuit. So, the state moves to the next state at every rising edge of the clock signal

So, there is no label on the arrow. ⇒

The next-state table can be read off from the state diagram:

Note that we put Q_D before Q_{JK} because Q_D connects to Y_1 which is the MSB.

Current State Q_D	Q_{JK}	Next State Q_D^*	Q_{JK}^*
0	0	0	1
0	1	1	1
1	0	0	0
1	1	1	0

Now, we use the next-state table to find the excitation inputs of the FFs.

For D FF, this is easy. If we want Q_D^* on the next rising edge of the clock, we put Q_D^* as the input D of the FF.

Current State Q_D	Q_{JK}	Next State Q_D^*	Q_{JK}^*	Excitation D	J	K
0	0	0	1	0	1	X
0	1	1	1	1	X	0
1	0	0	0	0	0	X
1	1	1	0	1	X	1

To fill out this part, we use the excitation table for J-K FF:

Q	Q^*	J	K
0	0	0	X

This mean that if the JK FF is currently outputting 0 (i.e. $Q=0$), if we want it to

0	1	1	1	1	X	0
1	0	0	0	0	0	X
1	1	1	0	1	X	1

To fill out this part, we use the excitation table for J-K FF:

Q	Q^*	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

This mean that if the JK FF is currently outputting 0 (ie. $Q=0$), if we want it to output 0 again ($Q^*=0$) on the next clock cycle, we need to set the J and K inputs of the FF to be either

$J=0$, $K=0$ (Hold mode)

or

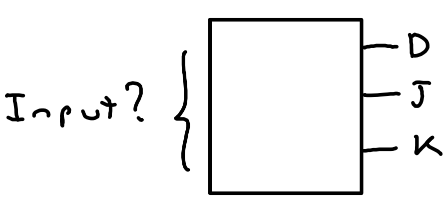
$J=0$, $K=1$ (RESET mode).

because K can be both 0 or 1 as long as $J=0$, we write $J=0$, $K=X$ in the excitation table.

The 1st row of the table above can be interpreted as followed:

To have the state changed from 00 to 01, we need to put $D=0$, $J=1$, $K=X$ into the FFs.

We need to build one more circuit to control the D, J, K so that they agree with the above table. This means we have one more box inside our machine which output D, J, K as shown.

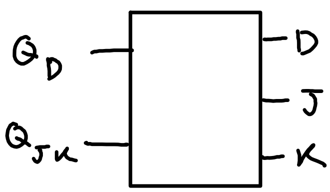


What should be the input(s) of this box?

Note that D, J, K are used to tell the FFs what should be the next state values. So, the box that we are working on right now is the box that calculate the next state value

(For D FF, the D is directly the value of the next output.)

Recall that the next state is determined by current state and input of the machine. In this question, there is no input. So, we determine the next state from the current state. Hence, the input to our box above is simply Q_D and Q_{JK} (the current state values) as shown below:

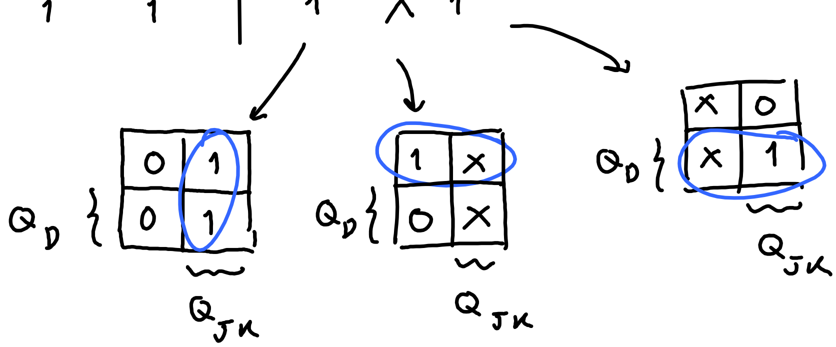


Note that this is simply a box that turn Q_D and Q_{JK} directly into D, J, K.

So, it is simply a combinational logic circuit. (pre-midterm material)

The truth table of this box can be taken out directly from the table above.

Inputs of the box		Outputs of the box.		
Q_D	Q_{JK}	D	J	K
0	0	0	1	X
0	1	1	X	0
1	0	0	0	X
1	1	1	X	1



The K-maps show that $D = Q_{JK}$

The K-maps show that

$$D = Q_{JK}$$

$$J = \overline{Q_D}$$

$$K = Q_D$$

Therefore, our final answer is